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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,056	03/30/2004	Masahiro Ito	Q80548	1303

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EXAMINER

SITTA, GRANT

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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11/20/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/812,056

Applicant(s)

ITO ET AL.

Examiner

Grant D. Sitta

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 9 is/are allowed.
- 6) ☐ Claim(s) 1-5, 7 and 8 is/are rejected.
- 7) ☐ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date See Continuation Sheet.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :9/8/2006,5/4/2006 and 3/30/2004.

DETAILED ACTION

Claim Objections

1. Examiner suggest claim 1 to read:
2. A video processor comprising: a bit rate converter for converting an M-bit input video signal to an N-bit output video signal by retaining grayscale levels wherein N is smaller than M; and

a gamma correction memory in which a plurality of N-bit input grayscale levels are mapped to a plurality of K-bit output grayscale levels which are distributed on a non-linear curve corresponding to a non-linear curve on which grayscale levels of a display device are distributed, **when said N-bit output video signal of said bit rate converter corresponds to one of the plurality of N-bit input grayscale levels,**

said gamma correction memory delivering one of the plurality of K-bit output grayscale levels to said display device.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Atsushi (JP Publication number 2002-221950) hereinafter Atsushi.

1. In regards to claim 1, Atsushi teaches a bit rate converter for converting (fig. 1 (10)) an M-bit input (fig. Input into 10) video signal to an N-bit (fig. 1 output of 10) output video signal by retaining grayscale levels (0068-0071), wherein N is smaller than M (0071); and a gamma correction memory (fig. 1 (11)) in which a plurality of N-bit input grayscale levels are mapped (fig. 8) to a plurality of K-bit output grayscale levels which are distributed (0073-0076) on a non-linear curve (fig. 8) corresponding to a non-linear curve on which grayscale levels (0082) of a display device are distributed, said gamma correction memory (fig. 1 (11)) delivering one of the plurality of K-bit output grayscale levels to said display device when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10)) corresponds to one of the plurality of N-bit input grayscale levels (0071-0082).

2. In regards to claim 3, Atsushi teaches wherein said K-bit output grayscale levels value, are interpolated grayscale levels of the N-bit input grayscale levels (0071-0073).

3. In regards to claim 4, Atsushi teaches wherein K is equal to M (0082) and (fig. 1 (12)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi in view of Lumelsky et al (5,196,924) hereinafter, Lumelsky,

6. In regards to claim 2, Atsushi discloses the limitations of claim 1,

Atsushi differs from the claimed invention in that Atsushi does not disclose wherein K is equal to N.

However, Lumelsky discloses K is equal to N. (col. 5, lines 25-25)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Lumelsky to include the use of K is equal to N as taught by Lumelsky in order to further conserve memory.

7. In regards to claim 5, comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits (col. 6, lines 1-46).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi, in view of Lu et. al (US 7,085,016) hereinafter, Lu.

9. In regards to claim 7, Atsushi discloses the limitations of claim 1,

Atsushi differs from the claimed invention in that Atsushi does not explicitly disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits.

However, Lu teaches a system and method for wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits (fig. 1 col. Col. 2, lines 57-67).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi to include the use of dithering as taught by Lu in order to select a dither reference as stated in (col. 2, lines 1-33).

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10. In regards to claim 8, Lu teaches an adder (fig. 5 (24)) for a binary-1 to higher N bits of the M-bit input video signal; a multiplexer (fig. 5 (23)) for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal (col. 3, lines 37-60); and a comparator (fig. 5 (22)) for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value (col. 5-6, lines 37-25).

Allowable Subject Matter

11. Claim 9 is allowed because the prior art does not contain. A bit rate converter comprising an input register for receiving an M-bit input video signal; a first adder for adding a binary-1 to a least significant bit position of a higher N bits of the M-bit input video signal; a first multiplexer for selecting an output of said first adder or said higher N bits in response to a first control signal; a first frame memory for storing an output of said first multiplexer; a second adder for adding a binary-1 to an output of the first frame memory; a second multiplexer for selecting an output of said second adder or an output of said first frame memory in response to a second control signal; a second frame memory for storing an output of said second multiplexer; a third adder for adding a binary-1 to an output of the second frame memory; a third multiplexer for selecting an output of said third adder or an output of said second frame memory in response to a third control signal; a third frame memory for storing an output of said third multiplexer; and controller producing said first control signal only, said first and second control

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signals simultaneously, or said first, second and third control signals simultaneously, depending on truncated lower significant bits of the M-bit video signal.

12. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not contain a bit rate converter comprises: a first adder for a binary-1 to the least significant bit position of higher N bits of the M-bit input video signal; a first multiplexer for selecting an output of said first adder or said higher N bits in response to a first control signal; a first frame memory for storing an output of said first multiplexer; a second adder for, a binary-1 to an output of the first frame memory; a second multiplexer for selecting an output of said second adder or an output of said first frame memory in response to a second control signal; a second frame memory for storing an output of said second multiplexer; a third adder for summing a binary-1 to an output of the second frame memory; a third multiplexer for selecting an output of said third adder or an output of said second frame memory in response to a third control signal; a third frame memory for storing an output of said third multiplexer; and control means for producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on the truncated lower significant bits.

Response to Arguments

13. Applicant's arguments, Response to Arguments, filed 8/31/2007, with respect to the rejection(s) of claim(s) 1-8 under Shigeta have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Atsushi.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

November 6, 2007


AMARE MENGISTU
SUPERVISORY PATENT EXAMINER